



**PRODUCT/PROCESS
CHANGE NOTIFICATION**

PCN AMG/16/9830

Analog & MEMS Group (AMG)

**New material set in ST Bouskoura for General Purpose Analog
Automotive grade products in SO8 and SO14 packages**

WHAT:

Progressing on the activities related to quality continuous improvement, ST is glad to announce a new material set for Automotive Grade version of General Purpose Analog products in SO8 and SO14 packages produced in ST Bouskoura.

Please find more information related to material change in the table here below (for all impacted products except TL431AIYDT and TL1431AIYDT).

Material	Current process	Modified process	Comment
Diffusion location	ST Ang Mo Kio (Singapore)/ UMC / ST Agrate	ST Ang Mo Kio (Singapore)/ UMC / ST Agrate	No change
Assembly location	ST Bouskoura	ST Bouskoura	No change
Molding compound	Sumitomo G700K	Sumitomo G700KC	Similar grade version more adapted to high density frame
Die attach	Ablestick 8601-S25	Ablestick 8601-S25	No change
Leadframe	Copper preplated NiPdAgAu standard density	Copper preplated ag spot High density	Move to Sn plating to solve some sporadic discoloration issues
Wire	Copper 1 mil	Copper 1 mil	No change
Plating	NiPdAgAu <i>(see comment on Moisture Barrier Bag)</i>	Sn	Sn plating already running for standard product for more than 3 year on SO package and will allow to solve sporadic discoloration issues seen on NiPdAgAu plating

Please find more information related to material change for TL431AIYDT and TL1431AIYDT :

Material	Current process	Modified process	Comment
Diffusion location	ST Ang Mo Kio (Singapore)	ST Ang Mo Kio (Singapore)	No change
Assembly location	ST Bouskoura	ST Bouskoura	No change
Molding compound	HITACHI MP8000CH4-2A	Sumitomo G700KC	Move to a high reliability compound with lower moisture absorption and less ionic content
Die attach	HITACHI EN4900 ST10	Ablestick 8601-S25	Will allow to solve some sporadic inhomogeneity issues seen on current glue
Leadframe	Copper preplated NiPdAu standard density	Copper preplated ag spot High density	Move to Sn plating to solve some sporadic discoloration issues
Wire	Gold 1 mil	Copper 1 mil	For production standardisation
Plating	NiPdAgAu <i>(see comment on Moisture Barrier Bag)</i>	Sn	Sn plating already running for standard product for more than 3 year on SO package and will allow to solve sporadic discoloration issues seen on NiPdAgAu plating
MSL	1	3	As per internal rules for leadframe with fused pins

Moisture barrier bag on NiPdAgAu plating frame products :

Please note that we will start on the current process (with NiPdAgAu plating) the implementation of a Moisture Barrier Bag from WK23'2016. This bag will protect the product during exposure to uncontrolled environment before product usage (transportation/storage) and will avoid any lead coloration variation.

The Moisture Barrier Bag will contain desiccant. The Label will be positioned on the MBB. Once the MBB is removed, there is no change as the reel has a label too.

This moisture barrier bag will be removed once we switch to the new material set (with Tin plating) as it won't be sensitive to lead discoloration anymore.

For more details, please refer to the appendix at the end of this document.

Samples of vehicle test are available now and other samples will be launched upon customer's requests. Please submit requests for samples within 30 days of this notification.

WHY:

This material change will contribute to ST's continuous quality product improvement and ensure a consistent assembly process through all the SO production lines.

HOW:

The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:

The new material set will be implemented in Q3/2016 in Bouskoura.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The second level interconnect, printed on label will move from e4 to e3.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.

There is -as well- no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

Shipments may start earlier with the customer's written agreement.

Reliability Report

*New Halogen free material set for SO in
ST Bouskoura for Automotive products*

General Information		Locations	
Product Line	0393, 0339, 0084, UW23,0924, UY44, UY18,16VA,0912, V912	Wafer fab	ST Singapore ST Agrate, UMC
Product Description	Dual comparator, bipolar, Quad comparator bipolar, quad Jfet op amp, Protected Trasmit At Up To 12 Mb , quad op amp, CMOS quad and dual comparator, 5V Supervisor, Dual op amp	Assembly plant	ST Bouskoura (Morocco)
P/N	LM2903YDT, LM2901YDT, TL084IYDT, ST3485EIYDT, TS924IDT, TSX3704IYDT, TSX3702IYDT, STM706YM7F, TS912IYDT, TV912IYDT	Reliability Lab	ST Grenoble, ST Bouskoura
Product Group	AMG		
Product division	General Purpose Analog &RF		
Package	SO8/14		
Silicon Process technology	Bipolar, Jfet , BCD3S, HF2CMOS, HVG8A, HCMOS4, HC1PA, HF5CMOS		

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

- To qualify a new material set for Automotive products in SO package produced in ST Bouskoura :
- Sumitomo G700KC which is an evolution of Sumitomo G700K
 - move from NiPdAgAu preplating to Sn postplating


3.2 Conclusion

Qualification Plan requirements have been fulfilled without issue. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

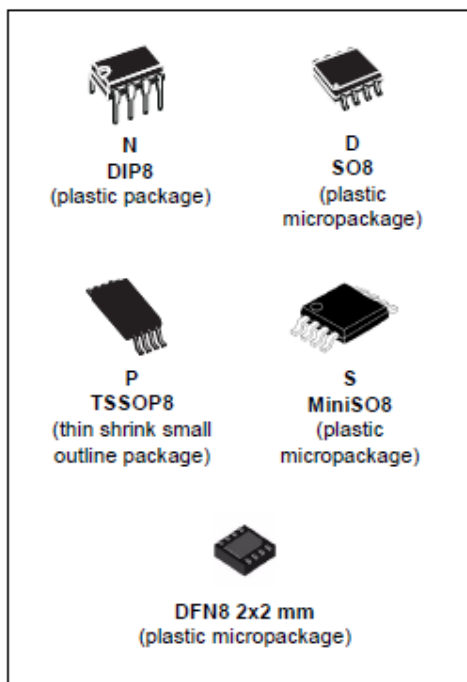
LM2903YDT


life.augmented

LM2903

Low-power dual voltage comparator

Datasheet - production data



- TTL, DTL, ECL, MOS, CMOS compatible outputs
- Automotive qualification

Related products

- See LM2903W for similar device with higher ESD performances
- See LM2903H for similar device with operating temperature up to 150 °C

Description

This device consists of two independent low-power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

In addition, the device has a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

Features

- Wide single supply voltage range or dual supplies +2 V to +36 V or ± 1 V to ± 18 V
- Very low supply current (0.4 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ± 5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. ($I_O = 4$ mA)
- Differential input voltage range equal to the supply voltage

LM2901YDT,



LM2901

Low-power quad voltage comparator

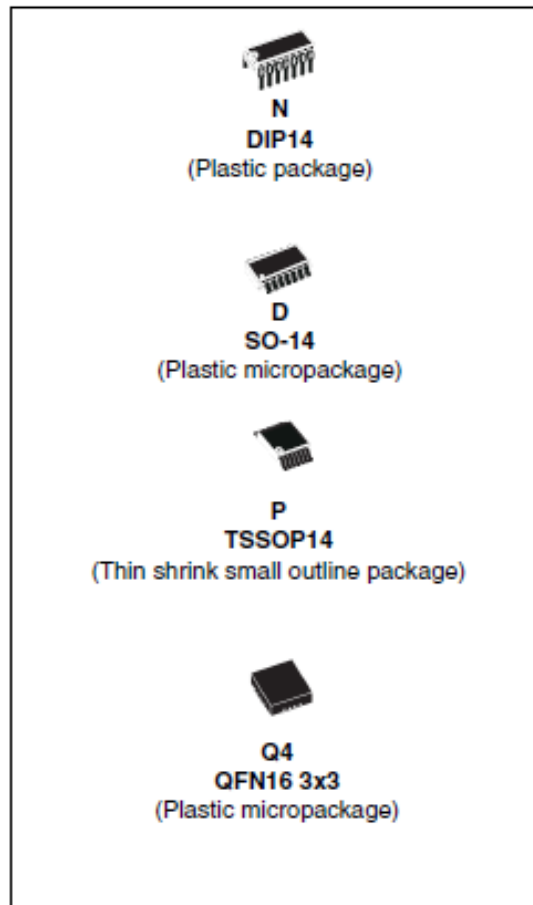
Features

- Wide single supply voltage range or dual supplies for all devices: +2 V to +36 V or ± 1 V to ± 18 V
- Very low supply current (1.1 mA) independent of supply voltage (1.4 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ± 5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. ($I_O = 4$ mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs

Description

This device consists of four independent precision voltage comparators, which are designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.



TL084IYDT:



TL084, TL084A, TL084B

General purpose JFET quad operational amplifiers

Datasheet — production data

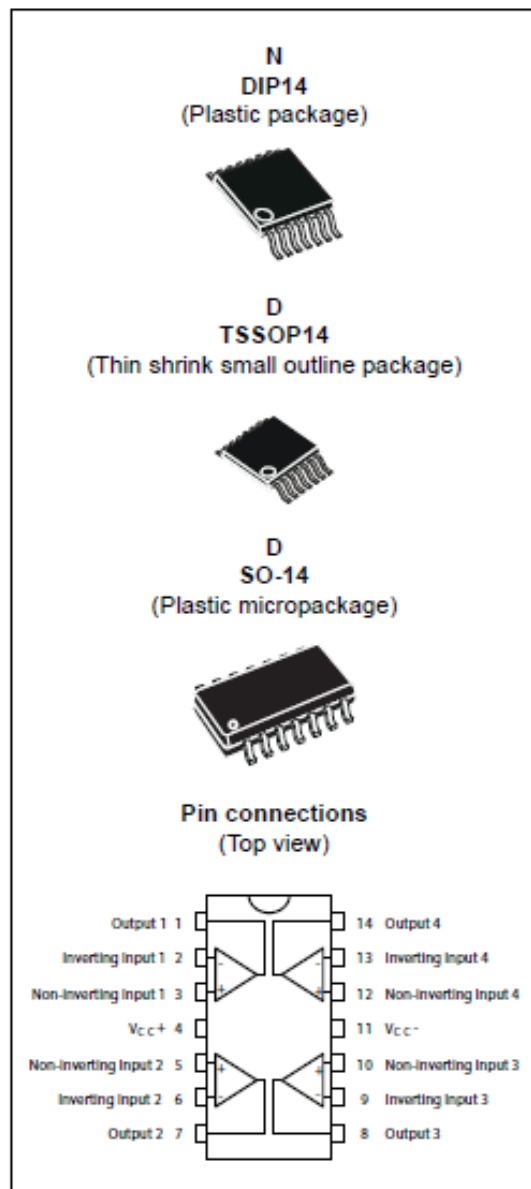
Features

- Wide common-mode (up to V_{CC}^+) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch up free operation
- High slew rate: 16 V/ μ s (typical)

Description

The TL084, TL084A, and TL084B are high-speed, JFET input, quad operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

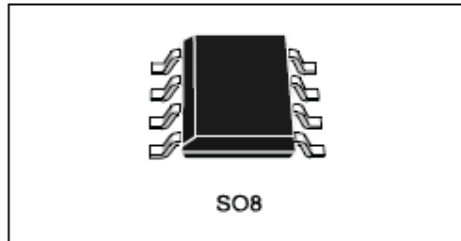




ST3485EB, ST3485EC, ST3485EIY

3.3 V powered, 15 kV ESD protected, up to 12 Mbps RS-485/
RS-422 transceiver

Datasheet - production data



Description

The ST3485EB/EC/EIY device is ± 15 kV ESD protected, 3.3 V low power transceiver for RS-485 and RS-422 communications. The device contains one driver and one receiver in half duplex configuration.

The ST3485E device transmits and receives at a guaranteed data rate of at least 12 Mbps.

All transmitter outputs and receiver inputs are protected to ± 15 kV IEC 61000-4-2 air discharge.

Driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high impedance state.

Table 1: Device summary

Order code	Temp range	Package	Packaging
ST3485ECDR	0 to 70 °C	SO8 (tape and reel)	2500 parts per reel
ST3485EBDR	-40 to 85 °C		
ST3485EIYDT	-40 to 125 °C		

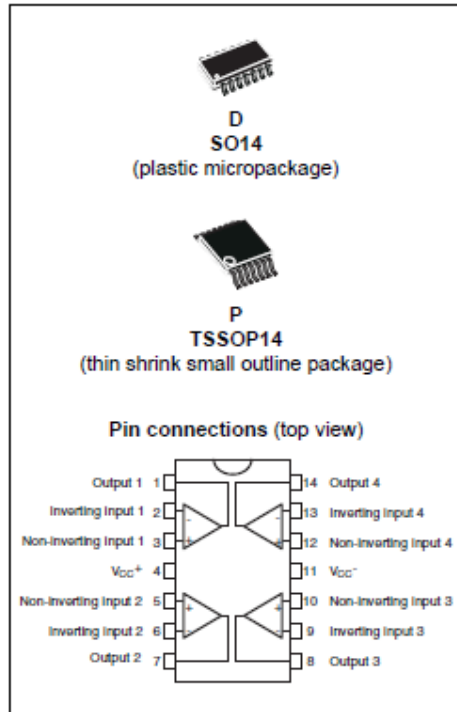
Features

- ESD protection
 - ± 15 kV IEC 61000-4-2 air discharge
 - ± 8 kV IEC 61000-4-2 contact discharge
- Operate from a single 3.3 V supply - no charge pump required
- Interoperable with 5 V logic
- 1 μ A low current shutdown mode max.
- Guaranteed 12 Mbps data rate
- -7 to 12 V common mode input voltage range
- Half duplex versions available
- Industry standard 75176 pinout
- Current limiting and thermal shutdown for driver overload protection
- Guaranteed high receiver output state for floating inputs with no signal present
- Allow up to 64 transceivers on the bus
- Available in SO8 package
- Automotive grade (ST3485EIY)

TS924, TS924A

Rail-to-rail output current quad operational amplifier

Datasheet - production data



- ESD internal protection: 3 kV
- Latch-up immunity
- Macromodel included in this specification

Related products

- See the TS921 device for the single version and the TS922 device for the dual version
- See the TSX56x series for smaller packages

Applications

- Headphone amplifiers
- Piezoelectric speaker drivers
- Sound cards
- MPEG boards, multimedia systems
- Line drivers, buffers
- Cordless telephones and portable communication equipment
- Instrumentation with low noise as key factor

Description

The TS924 and TS924A devices are rail-to-rail quad BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation.

High output current allows low load impedances to be driven.

The TS924 and TS924A devices exhibit a very low noise, low distortion, low offset, and high output current capability, making these devices an excellent choice for high-quality, low-voltage, and battery-operated audio systems.

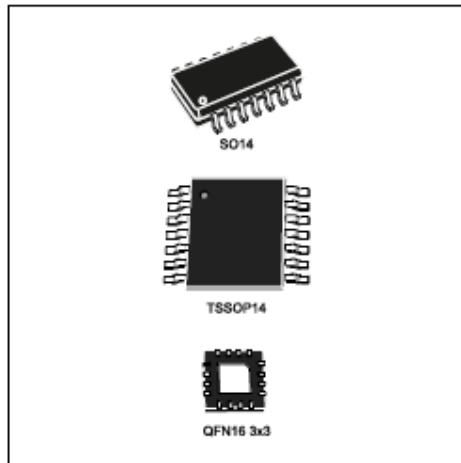
The devices are stable for capacitive loads up to 500 pF.

Features

- Rail-to-rail input and output
- Low noise: 9 nV/ $\sqrt{\text{Hz}}$
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1.3 V/ μs
- Operating range from 2.7 V to 12 V
- Low input offset voltage: 900 μV max. (TS924A)

Micropower quad CMOS voltage comparators

Datasheet - production data



Related products

- Pin-to-pin and functionally compatible with the dual CMOS TS3704 comparators
- See TSX339 for open drain output

Applications

- Automotive
- Industrial

Description

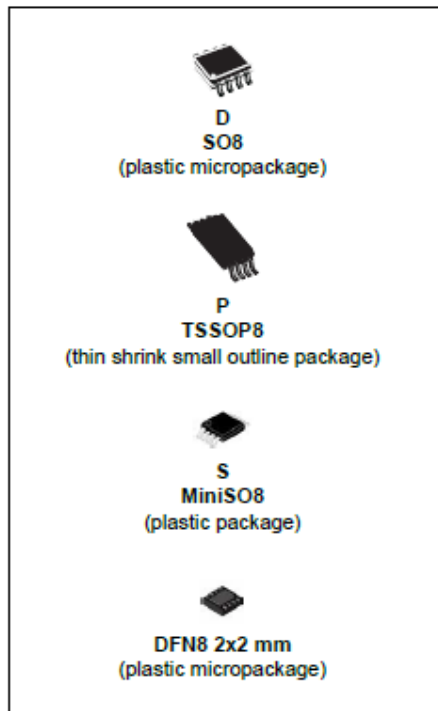
The TSX3704 is a micropower CMOS quad voltage comparator which exhibits a very low current consumption of 5 μ A typical per comparator. This device was designed as the improvement of the TS3704: it shows a lower current consumption, a better input offset voltage, and an enhanced ESD tolerance. The TSX3704 is fully specified over a wide temperature range and is proposed in automotive grade for the TSSOP14 package. It is fully compatible with the TS3704 CMOS comparator and is available with similar packages. The new tiny package, QFN16 3x3, is also proposed for the TSX3704 thus allowing even more integration on applications.

Features

- Low supply current: 5 μ A typ. per comparator
- Wide single supply range 2.7 V to 16 V or dual supplies (± 1.35 V to ± 8 V)
- Extremely low input bias current: 1 pA typ.
- Input common-mode voltage range includes ground
- Push-pull output
- High input impedance: 10^{12} Ω typ
- Fast response time: 2.7 μ s typ. for 5 mV overdrive
- ESD tolerance: 4 kV HBM, 200 V MM

Micropower dual CMOS voltage comparators

Datasheet - production data

**Features**

- Low supply current: 5 μ A typ. per comparator
- Wide single supply range 2.7 V to 16 V or dual supplies (± 1.35 V to ± 8 V)
- Extremely low input bias current: 1 pA typ.

- Input common-mode voltage range includes ground
- Push-pull output
- High input impedance: 10^{12} Ω typ
- Fast response time: 2.7 μ s typ. for 5 mV overdrive
- ESD tolerance: 4 kV HBM, 200 V MM

Related products

- Pin-to-pin and functionally compatible with the dual CMOS TS3702 comparators
- See the TSX393 for open drain output

Applications

- Automotive
- Industrial

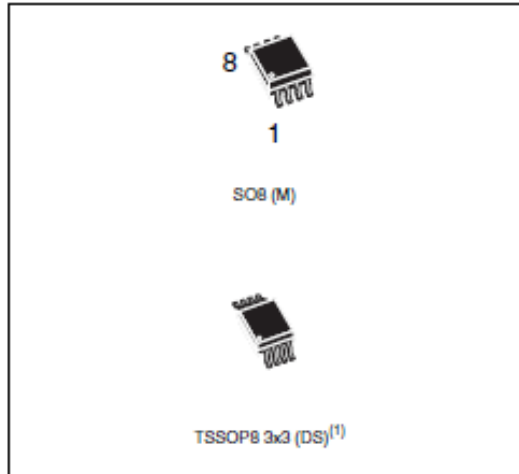
Description

The TSX3702 is a micropower CMOS dual voltage comparator which exhibits a very low current consumption of 5 μ A typical per comparator. This device was designed as the improvement of the TS3702: it shows a lower current consumption, a better input offset voltage, and an enhanced ESD tolerance. The TSX3702 is fully specified over a wide temperature range and is proposed in automotive grade for the SO8 package. It is fully compatible with the TS3702 CMOS comparator and is available with similar packages. New tiny packages (MiniSO8 and DFN8 2x2 mm) are also proposed for the TSX3702 thus allowing even more integration on applications.

STM705, STM706 STM707, STM708, STM813L

5 V supervisor

Datasheet - production data



- 200 ms (typ) t_{rec}
- Watchdog timer - 1.6 s (typ)
- Manual reset input (\overline{MR})
- Power-fail comparator (PFI/ \overline{PFO})
- Low supply current - 40 μ A (typ)
- Guaranteed \overline{RST} (RST) assertion down to $V_{CC} = 1.0$ V
- Operating temperature:
 - 40 °C to 85 °C (industrial grade) or
 - 40 °C to 125 °C (automotive grade for the STM706 only)
- RoHS compliance
 - Lead-free components are compliant with the RoHS directive

1. Contact local ST sales office for availability.

Features

- 5 V operating voltage
- Precision V_{CC} monitor
 - STM705/707/813L
 - $4.50 \text{ V} \leq V_{RST} \leq 4.75 \text{ V}$
 - STM706/708
 - $4.25 \leq V_{RST} \leq 4.50 \text{ V}$
- RST and \overline{RST} outputs

Table 1. Device summary

	Watchdog input	Watchdog output ⁽¹⁾	Active-low \overline{RST} ⁽¹⁾	Active-high RST ⁽¹⁾	Manual reset input	Power-fail comparator
STM705	✓	✓	✓		✓	✓
STM706 ⁽²⁾	✓	✓	✓		✓	✓
STM707			✓	✓	✓	✓
STM708			✓	✓	✓	✓
STM813L	✓	✓		✓	✓	✓

1. Push-pull output

2. Automotive grade (-40 °C to 125 °C) option for the STM706 only.

4.2 Construction note

	P/N LM2903YDT	P/N LM2901YDT	P/N TL0841YDT	P/N ST3485E1YDT	P/N TS9241DT
Wafer/Die fab. information					
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Technology	Bipolar	Bipolar	JFet	BCD3S	HF2CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	950 x 870 µm	1370x1270	2480 x 1460	1950x2720	1980x2450
Bond pad metallization layers	AlSiCu	AlSiCu	AlSiCu	AlSi	AlSiCu
Passivation type	Nitride	Nitride	P-VAPOX/NITRIDE	P-VAPOX/NITRIDE/POLYIMIDE	P-VAPOX/NITRIDE
Wafer Testing (EWS) information					
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information					
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO14	SO14	SO8	SO14
Molding compound	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin
Final testing information					
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K

	P/N TSX3704YDT	P/N TSX37021YDT	P/N STM706YM7F	P/N MC33079YDT	P/N TS9121YDT	P/N TSV9121YDT
Wafer/Die fab. information						
Wafer fab manufacturing location	ST Agrate	ST Agrate	ST Singapore	ST Singapore	ST Singapore	UMC
Technology	HVG8A	HVG8A	HCMOS4	Bipolar	HC1PA	HF5CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	1830x1440 µm	1018x1238 µm	1350 x 1510µm	3230x1950µm	2600x1950µm	1100x1070µm
Bond pad metallization layers	AlCu	AlCu	AlSiCu	AlSiCu	AlSi	AlCu
Passivation type	HDP/TEOS/SiN/Polyimide	HDP/TEOS/SiN/Polyimide	PSG+Silicon Nitride+Polyimide	Nitride	PVAPOX+Nitride	Nitride
Wafer Testing (EWS) information						
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information						
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO14	SO14	SO8	SO14	SO8	SO8
Molding compound	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin
Final testing information						
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	Bipolar/SO8	0393	CZ53005LRP CZ53005LRN CZ53005LRQ CZ53005LRR CZ53005LRM CZ53005LRL
2	Bipolar/SO14	0339	CZ52405FR6 CZ52405FR7 CZ52405FR8
3	JFet / So14	0084	CZ53306W
4	BCD3S/SO8	UW23	CZ5430CN
5	HF2CMOS	0924	CZ5380CA01
6	HVG8A/SO14	UY44	CZ52501F01
7	HVG8A/SO14	UY18	CZ537088RM
8	HCMOS4/SO8	16VA	CZ53607S
9	Bipolar/SO14	3079	CZ5400CJRQ
10	HC1PA/SO8	0912	
11	HF5CMOS	V912	CZ5440C1RR

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1 0393	Lot 2 0339	Lot 3 0084	Lot 4 UW23	Lot5 0924	
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H	0/78	0/78		0/77*		* Tj=125°C
					500 H	0/78	0/78		0/77*		
					1000 H	0/78	0/78		0/77*		
ELFR	N	JESD22 A-008	Ta = 125°C, BIAS		0/450	0/450			0/350		
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	6X0/77	3x0/77	0/77	0/45	0/77	(1)
					500 H	6X0/77	3x0/77	0/77	0/45	0/77	
					1000 H	6X0/77	3x0/77	0/77	0/45	0/77	
					2000H		3x0/77				
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	6x0/77	3x0/77	0/77	0/77 0/77	0/77	(1)
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	6x0/77	3x0/77	0/77	0/77	0/77	(1)
					200 cy	6x0/77	3x0/77	0/77	0/77	0/77	
					500 cy	6x0/77	3x0/77	0/77	0/77	0/77	
					1000cy	6x0/77	3x0/77	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H		0/78		0/77		
					500 H		0/78		0/77		
					1000 H		0/78		0/77		
Other Tests											
ESD	N	AEC Q101- 001, 002 and 005	CDM			0/3	0/3	0/3			
SD	N		After ageing 8h and 16h			Pass	Pass	Pass	Pass		

(1) Additional split lot to cover the whole assembly variability

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						Note
						Lot 6 UY44	Lot 7 UY18	Lot8 16VA	Lot9 3079	Lot10 0912	Lot11 V912	
HTB/ HTOL	N	JESD22 A-108	Tj = 125°C, BIAS		168 H	0/77		0/77			0/77	
					500 H	0/77		0/77		0/77		
					1000 H	0/77		0/77		0/77		
ELFR	N	JESD22 A-008	Ta = 125°C, BIAS			450			0/450	450		
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/77	0/77	0/45	0/77			
					500 H	0/77	0/77	0/45	0/77			
					1000 H	0/77		0/45	0/77			
					2000H							
Package Oriented Tests												
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS				
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	0/77 0/77		0/77 0/77	0/77			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	0/77			
					200 cy	0/77	0/77	0/77	0/77			
					500 cy	0/77	0/77	0/77	0/77			
					1000cy			0/77	0/77			
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/77		0/77				
					500 H	0/77		0/77				
					1000 H	0/77		0/77				
Other Tests												
ESD	N	AEC Q101- 001, 002 and 005	CDM		1500V	0/3		0/3				
SD	N		After ageing 8h and 16h					PASS				

Statistical comparison of electrical parameters:

TS912IYDT

Limits	OQA 1FT 2WS	Mode	New molding compound G700KC		reference lot		Comment
			AVG	CPK	AVG	CPK	
P106_*0	lcc for one amp	mA	0.53	>1.66	0.48	>1.66	
P101_A0	Vio	mV	0.23	>1.66	0.04	>1.66	
P101_B0	Vio	mV	0.05	>1.66	-0.05	>1.66	
P106_*2	lcc	mA	0.18	>1.66	0.16	>1.66	
P101_A2	Vio	mV	0.33	>1.66	0.05	>1.66	
P101_B2	Vio	mV	0.09	>1.66	-0.09	>1.66	
P106_*9	lcc for one amp	uA	165.68	>1.66	150.29	>1.66	
P102_A1	lio	pA	-2.21	>1.66	1.16	>1.66	
P102_B1	lio	pA	-4.56	>1.66	5.64	>1.66	
P103_A1	libn	pA	9.83	>1.66	11.48	>1.66	
P103_B1	libn	pA	6.81	>1.66	-1.04	>1.66	
P103_A1	libp	pA	12.05	>1.66	10.31	>1.66	
P103_B1	libp	pA	11.37	>1.66	-6.68	>1.66	
P109_A2	cmr	dB	81.65	not gaussian	82.61	not gaussian	
P109_B2	cmr	dB	81.14	not gaussian	82.36	not gaussian	
P109_A1	cmr	dB	97.29	not gaussian	96.86	not gaussian	
P109_B1	cmr	dB	97.33	not gaussian	96.73	not gaussian	
P109_A3	cmr	dB	71.60	not gaussian	72.38	not gaussian	
P109_B3	cmr	dB	71.03	not gaussian	72.00	not gaussian	
P105_A2	SVR	dB	83.29	not gaussian	82.64	not gaussian	
P105_B2	SVR	dB	82.67	not gaussian	82.89	not gaussian	
P105_A1	SVR	dB	96.35	not gaussian	95.77	not gaussian	
P105_B1	SVR	dB	96.69	not gaussian	95.93	not gaussian	
P104_A1	Avd	V/mV	64.78	not gaussian	65.21	not gaussian	
P104_B1	Avd	V/mV	109.18	not gaussian	80.31	not gaussian	
P104_A2	Avd	V/mV	16.58	not gaussian	14.58	not gaussian	
P104_B2	Avd	V/mV	18.51	not gaussian	16.18	not gaussian	
P117_A5	Voh	V	9.99	>1.66	9.99	>1.66	
P117_B5	Voh	V	9.99	>1.66	10.00	>1.66	
P117_A5	Vol	V	0.03	>1.66	0.03	>1.66	
P117_B5	Vol	V	0.03	>1.66	0.01	>1.66	
P117_A3	Voh	V	2.96	>1.66	2.97	>1.66	
P117_B3	Voh	V	2.96	>1.66	2.97	>1.66	

P117_A3	Vol	V	0.03	>1.66	0.03	>1.66	
P117_B3	Vol	V	0.03	>1.66	0.03	>1.66	
P117_A4	Voh	V	2.64	>1.66	2.67	>1.66	
P117_B4	Voh	V	2.64	>1.66	2.67	>1.66	
P117_A4	Vol	V	0.25	>1.66	0.24	>1.66	
P117_B4	Vol	V	0.25	>1.66	0.24	>1.66	
P137_A2	Isk	mA	39.98	>1.66	41.11	>1.66	
P137_B2	Isk	mA	41.05	>1.66	41.85	>1.66	
P137_A2	Isr	mA	-40.47	>1.66	-40.49	>1.66	
P137_B2	Isr	mA	-40.32	>1.66	-40.97	>1.66	
P137_A1	Isk	mA	68.90	>1.66	77.90	>1.66	
P137_B1	Isk	mA	68.31	>1.66	77.29	>1.66	
P137_A1	Isr	mA	-62.56	>1.66	-70.97	>1.66	
P137_B1	Isr	mA	-66.33	>1.66	-74.66	>1.66	
P121_A2	GBP	MHz	0.93	>1.66	0.87	>1.66	
P121_B2	GBP	MHz	0.83	>1.66	0.78	>1.66	
P121_A1	GBP	MHz	1.44	>1.66	1.30	>1.66	
P121_B1	GBP	MHz	1.36	>1.66	1.27	>1.66	
P113_A2	SRn	V/uS	0.47	>1.66	0.41	>1.66	
P113_B2	SRn	V/uS	0.47	>1.66	0.41	>1.66	
P113_A2	SRp	V/uS	0.71	>1.66	0.61	>1.66	
P113_B2	SRp	V/uS	0.55	>1.66	0.48	>1.66	

LM2901YDT

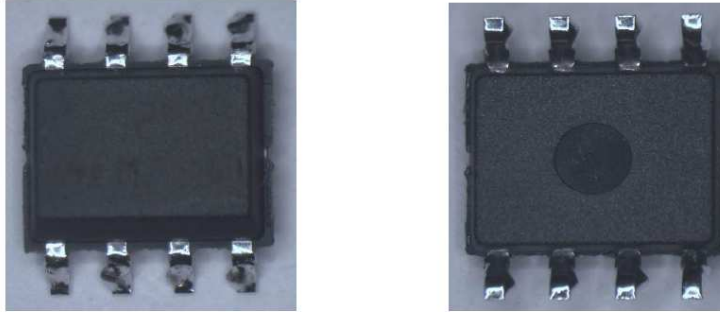
Limits	OQA 1FT 2WS	Units	New material set		reference		Comment
			AVG	CPK	AVERAGE	CPK	
P101_A0	Vio 5V	mV	-0.28	>1.6	-0.46	>1.6	
P101_B0	Vio 5V	mV	0.65	>1.6	0.40	>1.6	
P101_C0	Vio 5V	mV	-0.45	>1.6	-0.41	>1.6	
P101_D0	Vio 5V	mV	0.71	>1.6	0.52	>1.6	
P102_A1	lio 30V	nA	-2.61	>1.6	-1.87	>1.6	
P102_B1	lio 30V	nA	-3.24	>1.6	-4.50	>1.6	
P102_C1	lio 30V	nA	1.66	>1.6	-0.38	>1.6	
P102_D1	lio 30V	nA	-1.63	>1.6	2.13	>1.6	
P103_A1	libn 30V	nA	-31.90	>1.6	-29.23	>1.6	
P103_B1	libn 30V	nA	-27.01	>1.6	-30.42	>1.6	
P103_C1	libn 30V	nA	-30.00	>1.6	-27.22	>1.6	
P103_D1	libn 30V	nA	-31.15	>1.6	-25.55	>1.6	
P103_A1	libp 30V	nA	-29.29	>1.6	-27.36	>1.6	
P103_B1	libp 30V	nA	-23.76	>1.6	-25.92	>1.6	
P103_C1	libp 30V	nA	-31.66	>1.6	-26.84	>1.6	
P103_D1	libp 30V	nA	-29.52	>1.6	-27.68	>1.6	
P101_A4	Vio 30V 28.5V	mV	-0.46	>1.6	-0.55	>1.6	
P101_B4	Vio 30V 28.5V	mV	1.33	>1.6	0.97	>1.6	
P101_C4	Vio 30V 28.5V	mV	-0.81	>1.6	-0.86	>1.6	
P101_D4	Vio 30V 28.5V	mV	1.11	>1.6	0.86	>1.6	
P106_*1	lcc 5V	mA	0.24	>1.6	0.24	>1.6	
P106_*2	lcc 30V	mA	0.29	>1.6	0.29	>1.6	
P117_A1	Vol 5V	V	0.24	>1.6	0.22	>1.6	
P117_B1	Vol 5V	V	0.23	>1.6	0.20	>1.6	
P117_C1	Vol 5V	V	0.22	>1.6	0.20	>1.6	
P117_D1	Vol 5V	V	0.25	>1.6	0.22	>1.6	
P137_A1	lsk 5V	mA	18.37	>1.6	19.94	>1.6	
P137_B1	lsk 5V	mA	18.88	>1.6	20.38	>1.6	
P137_C1	lsk 5V	mA	18.55	>1.6	20.22	>1.6	
P137_D1	lsk 5V	mA	18.16	>1.6	19.52	>1.6	
P138_A1	loh 30V	uA	0.01	>1.6	0.02	>1.6	
P138_B1	loh 30V	uA	0.02	>1.6	0.01	>1.6	
P138_C1	loh 30V	uA	0.01	>1.6	0.01	>1.6	
P138_D1	loh 30V	uA	0.01	>1.6	0.01	>1.6	

Solderability:

Lot reference: CZ53005LRN,CZ53005LRQ, CZ53005LRR, CZ53005LRL

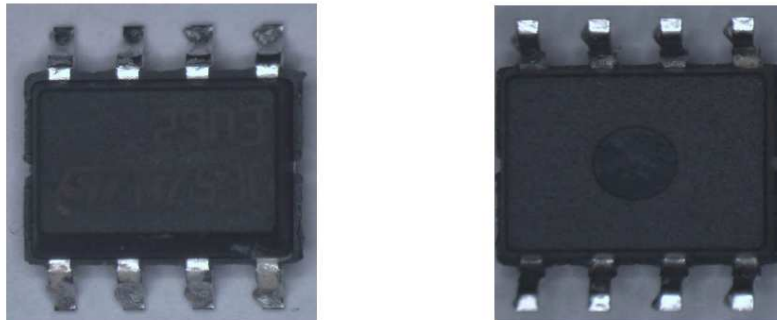
T0 solderability with SnPb bath and SnAgCu bath 0 reject on 15 units:

After SnPb



No solderability issue on all units after

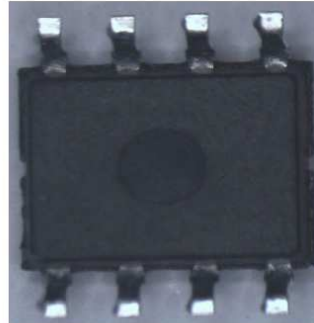
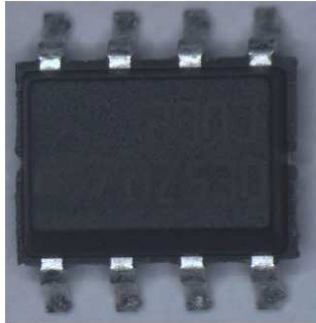
After SnAg



No solderability issue on all units after

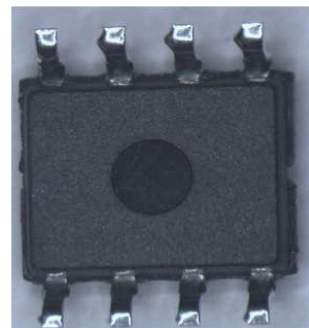
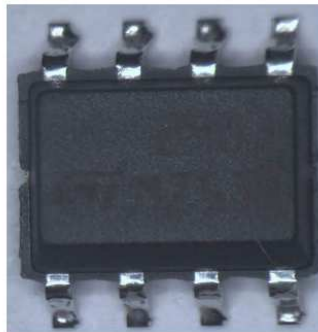
After 8h 85°C/85%RH solderability with SnPb bath and SnAgCu bath 0 reject on 15 units:

After SnAg



No solderability issue on all units after

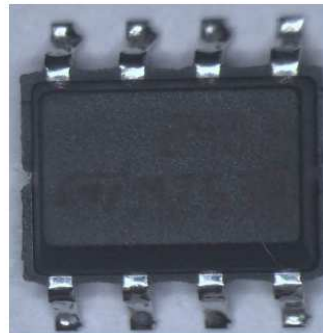
After SnPb



No solderability issue on all units after

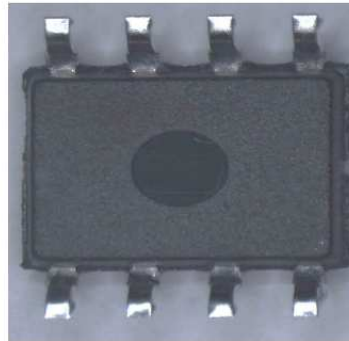
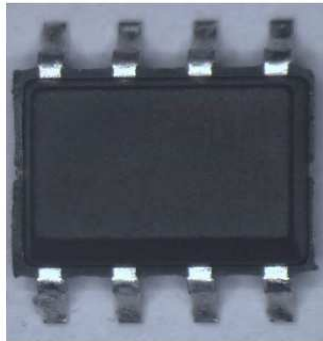
After 16h 150°C, solderability with SnPb bath and SnAgCu bath 0 reject on 15 units:

After SnPb



No solderability issue on all units after

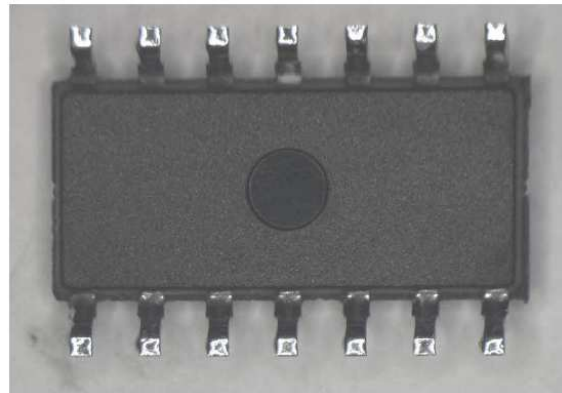
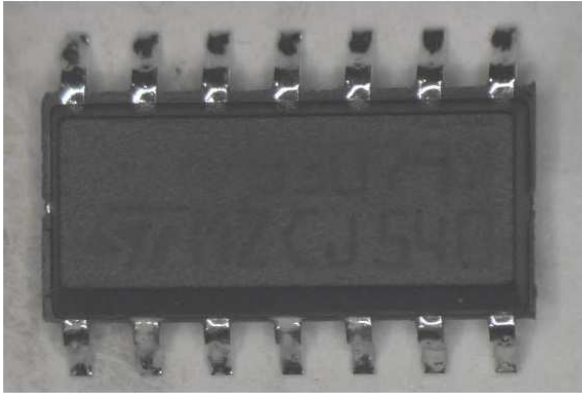
After SnAg
↓



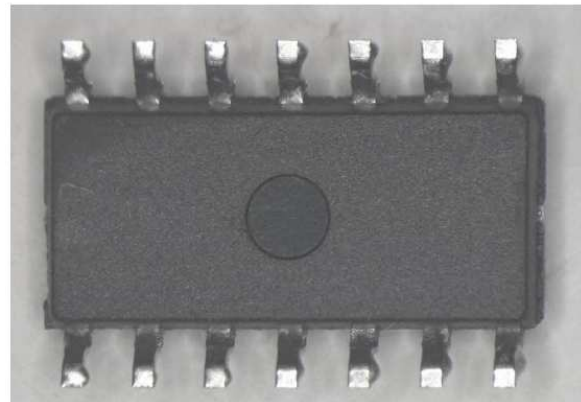
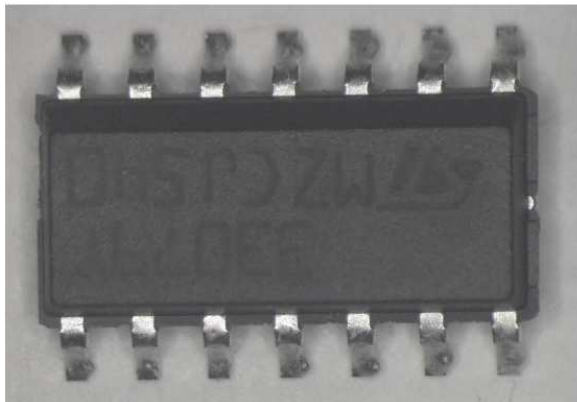
No solderability issue on all units after

Lot reference: CZ5400CJRQ
Line 3079
After 8h at 85°C / 85%RH

After SnPb



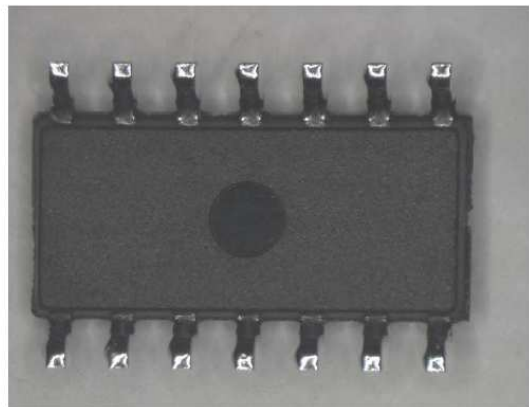
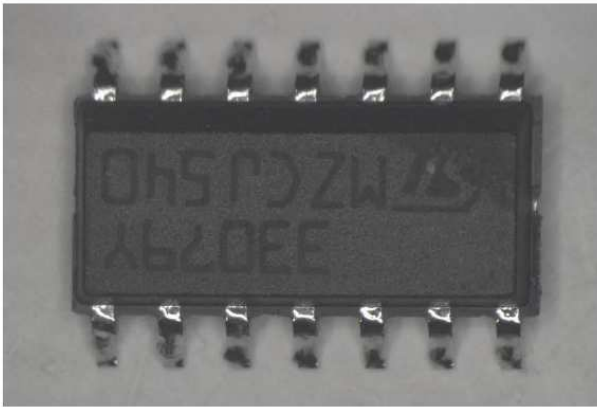
After SnAg



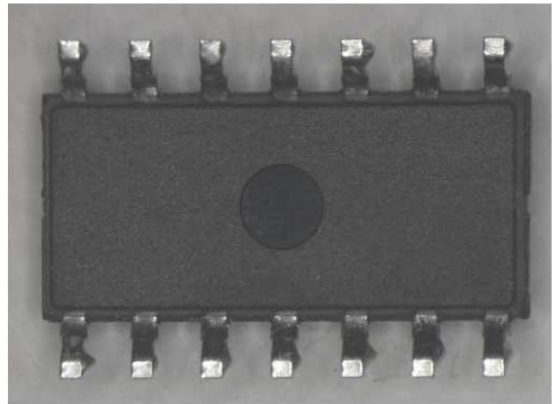
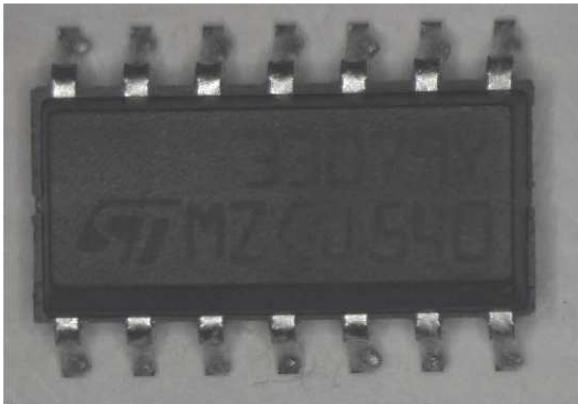
No solderability issue

After 16h at 150°C:

After SnPb



After SnAg



No solderability issue



**Tin Surface Finish Acceptance Testing
per JESD201 & JESD 22A121**

P. Crema

Assembled :
STM Marocco Bouskoura



SO8L PMOS

DISCLAIMER

The whisker test procedures identified in this report are used for determining the presence of tin whiskers and are performed by STMicroelectronics Inc., pursuant to current industry accepted JEDEC standards. The whisker test procedures used herein are unproven and may produce inconclusive results. STMicroelectronics Inc. makes no representation, warranty or guarantee of any kind with respect to the field performance, quality or freedom from whisker-related failures, of any package tested by STMicroelectronics using these procedures.

General Information



Package	SO8L <small>PMOS</small>
Factory	STMicroelectronics Morocco
Factory Location	Bouskoura
Lead Frame Alloy	Copper : O194
Lead Finish	Matte Tin
Tin Thickness	7 – 20 um on leads
Plating Vendor	Atotech <small>GmbH</small>
Plating Machine	MECO
Plating Chemistry	Stannopure HSM
Mitigation	Post Plating Bake within 24hrs @150 for 1 hr.

Chemical Plating process information



September 11 , 2008					
Description	Process	Volume tank (liter)	Make up Concentration (g/l or ml/l)	Density	Quantity used for the bath
Electro cleaner	Puronon RTR	80	100g/l		8kg
Activation Ni/Fe					
Activation Cu	Descabase Cu	80	50g/l		4kg
	H2SO4		30ml/l	1.61	3.36litre
Predip	MSA Special Acid HS	80	100ml/l	1.34	8litres
Tin plate	MSA Tin Solution HS 20	320	70g/l	1.53	81 litres
	MSA Special Acid HS		190 g/l	1.34	71 litres
	Stannopure HSM Additive HT		50ml/l	1	16litres
	Stannopure HSM Grain Refiner GF		15ml/l	1	4.8litres
	Antioxydant SN		5ml/l	1	1.6 litres
Neutral	Protectostan LF	80	100ml/l	1	8 litres
Stripper	Becastrip EL Part A	240	550ml/l	1.24	132 litres
	Becastrip EL Part B		20ml/l	1.53	4.8 litres

Plating equipment & process parameters



Equipment identification	Supplier	Type	Model
MECO 1	MECO	Continuous automatic plating	EPL 1200S



	Electro cleaner	Activation	Plating	Neutraliser
Temperature	50°C	RT	45°C	RT
Voltage /Ampère	50A	30A	120A 120A 120A 120A	-
Belt speed	4.0 m/mn			

Pre Conditions



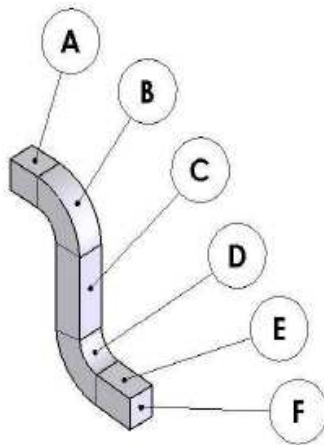
PreCondition	Conditions
No Pre condition	Ambient Only
Reflow (Single Pass)	215 deg C in air
Reflow (Single Pass)	245 – 260 deg C in air

Test plan 

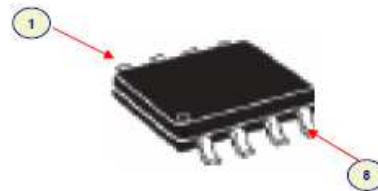
Test	Short description	Conditions
Thermal Cycling	TC	- 40°C to + 85°C
High Humidity Storage	HT	55°C-85%RH
Controlled Ambient Storage	RT	30°C-60%RH

Fig 1: Inspection Zones 

Inspection: Top + 2 Sides



Lead identification



Temp. Cycles Whiskers inspection results



Optical inspection @ 50 X						
Preconditioning	Device	Sample size	n. of cycles			
			@ 0	@ 500	@1000	@1500
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers
215°C	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers
247°C	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers

Soak 30c/60%RH Whisker Inspection Results



Optical inspection @ 50 X							
Preconditioning	Device	Sample size	Time in hrs				
			@ 0	@ 1000	@2000	@3000	@4000
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
215°C	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
247°C	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers

**Soak 55c/85%RH
Whisker Inspection Results**



Optical inspection @ 50 X								
			Time in hrs					
Preconditioning	Device	Sample size	@ 0	@ 1000	@2000	@3000	@4000	Discounted lead
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
215°C	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
247°C	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--

Wire strength

Dice 0924

	Ball shear	Wire pull
min	37.01	11.28
max	42.46	15.89
avg	39.80	13.48
std	1.90	1.30
cpk	2.85	2.42

Dice 3079

	Ball shear	Wire pull
min	36.35	12.24
max	43.93	16.83
avg	41.9475	14.11416667
std	1.762042494	1.143047523
cpk	2.66	2.95

Dice V912

	Ball Shear (g)	Wire Pull (g)
LSL	20	4
USL	56	--
Min	32.43	9.87
Max	39.14	13.22
Avg	35.31	11.73
Std	1.93	1.42
Cpk	2.64	1.81
Failure mode	AI	Wire, neck

Wire pull test results after TC
Dice 16VA

Wire Bonding Pull								
Cu wire 1 mils			Cu wire 1 mils			Cu wire 1 mils		
Nr.	value (gr)	failure mode	Nr.	value (gr)	failure mode	Nr.	value (gr)	failure mode
1	12.3	w ire break	11	9.7	neck ball	21	13.8	w ire break
2	12.3	neck ball	12	9.6	w ire break	22	13.5	w ire break
3	7.5	neck lead	13	11.9	w ire break	23	10.6	w ire break
4	12.3	neck lead	14	11.5	w ire break	24	12.3	w ire break
5	9.6	neck ball	15	11.9	w ire break	25	9.8	neck ball
6	9.1	neck lead	16	9.1	neck lead	26	10.4	neck lead
7	10.7	neck lead	17	10.8	neck lead	27	12.9	neck ball
8	7.9	neck lead	18	12.7	w ire break	28	10.5	neck lead
9	9.7	neck lead	19	10.3	neck ball	29	11.2	w ire break
10	12.8	neck lead	20	11.2	neck lead	30	10.9	w ire break

Average 11g, min 7.5g, max 13.8g

Die shear

Dice 3079

DA1	Die Shear (Kg)
USL	NA
LSL	1.58
Min	8.45
Max	10.09
Average	9.352
Stdev	0.62
Cpk	4.16

Dice 0393

	Die Shear (Kg)
USL	10
LSL	30
Min	6.92
Max	8.43
Average	7.82
Stdev	0.60
Cpk	3.24

Dice 0924

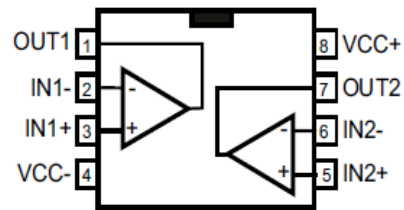
DA1	Die Shear (Kg)
USL	NA
LSL	1.21
Min	5.09
Max	7.4
Average	6.1576
Stdev	0.78
Cpk	2.12

6 ANNEXES

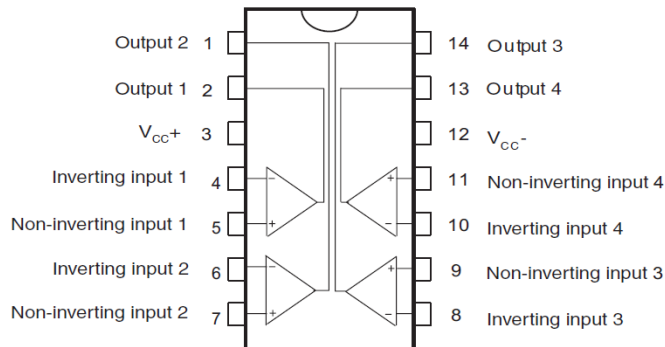
6.1 Device details

6.1.1 Pin connection

LM2903

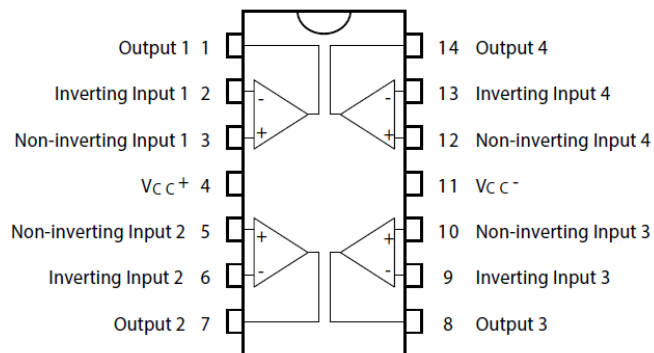


LM2901

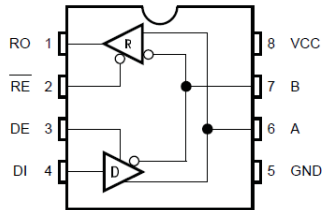


TL084

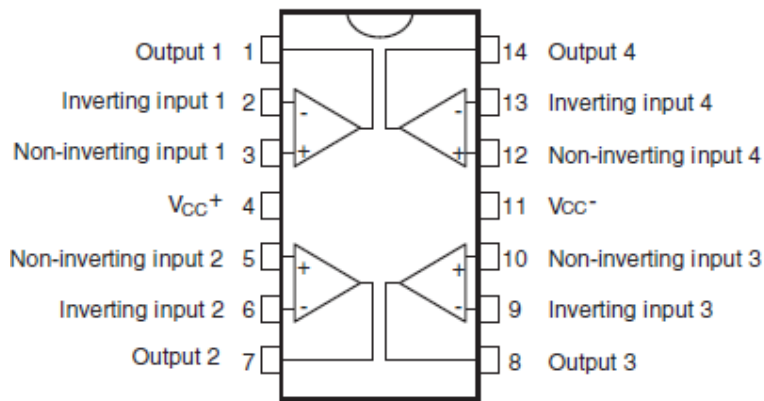
Pin connections (Top view)



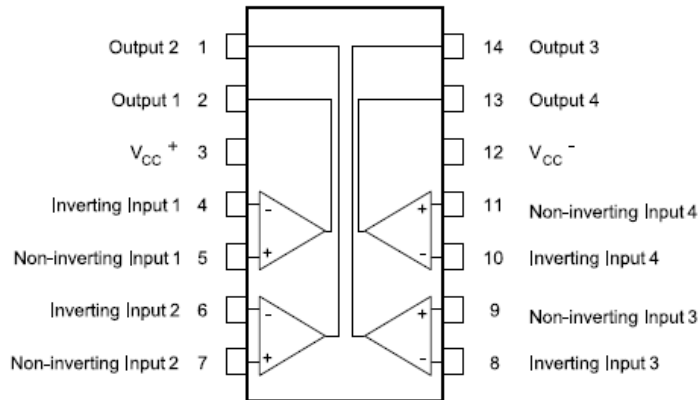
UW23



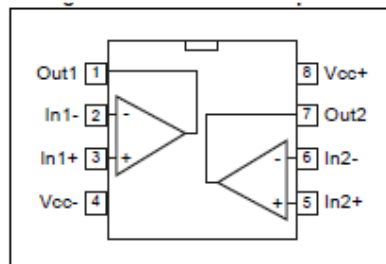
0924

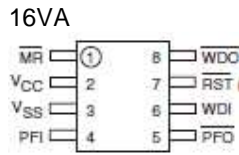


UY44



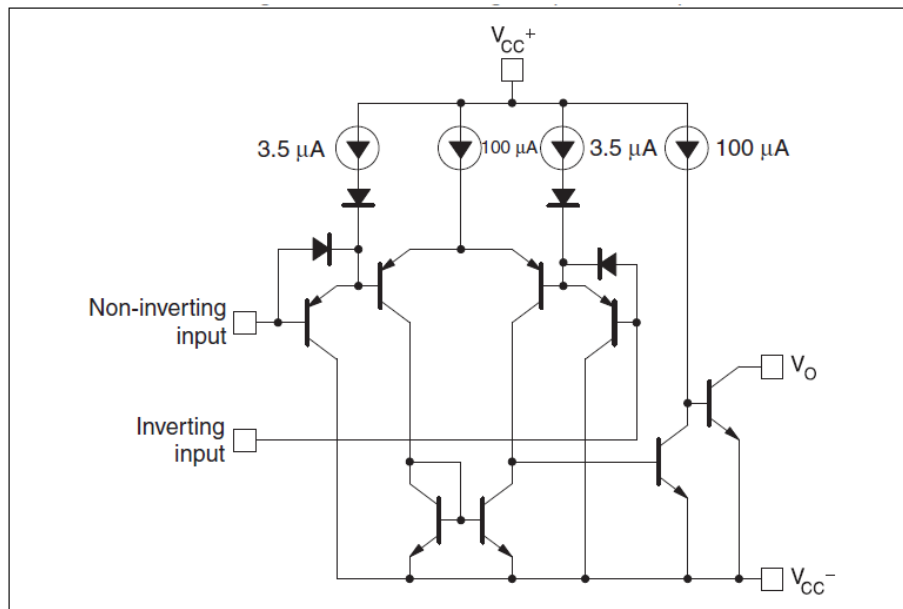
UY18



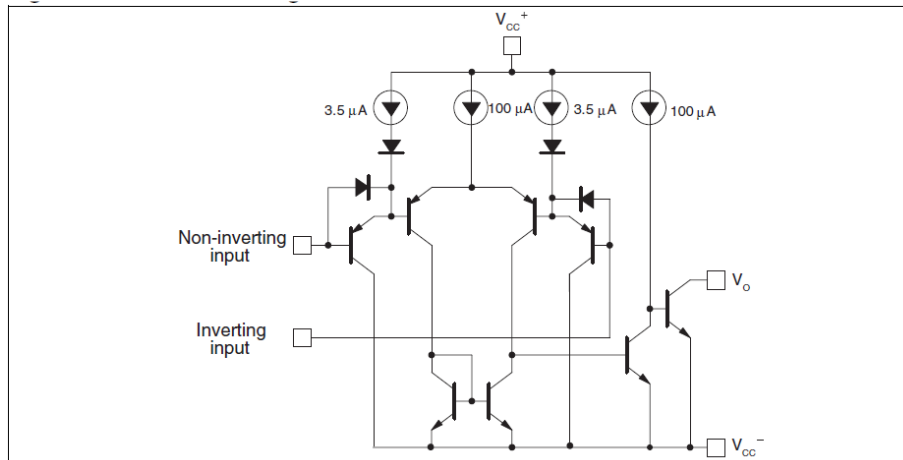


6.1.2 Block diagram

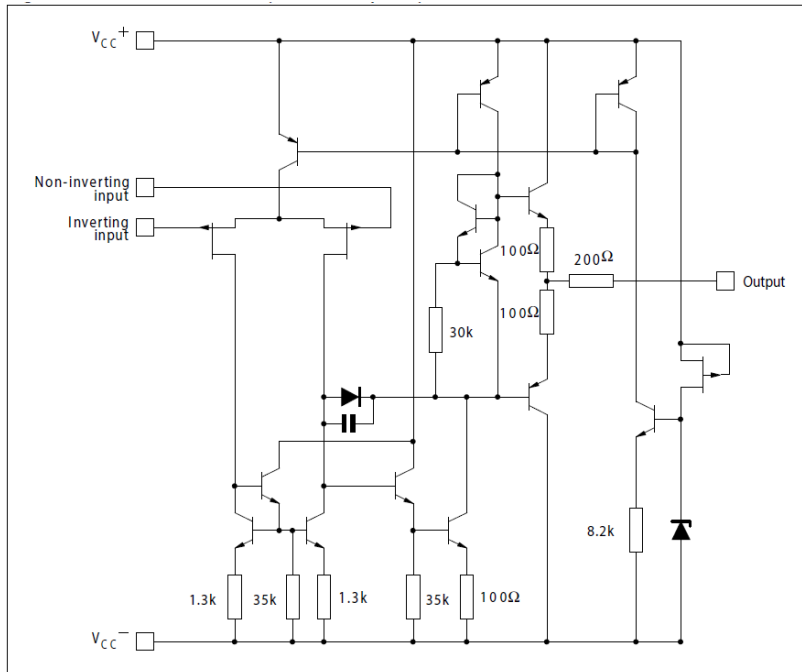
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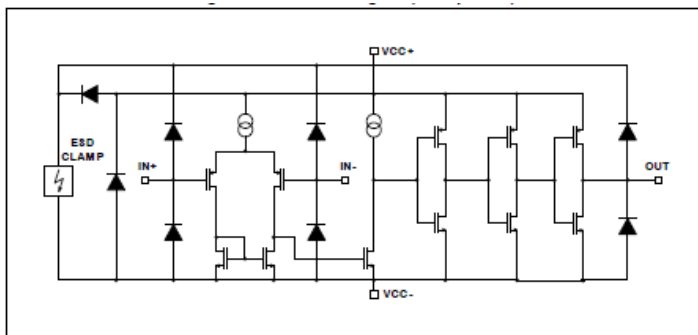
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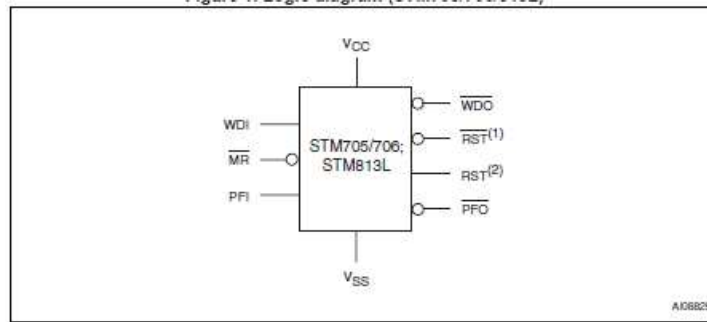
TL084



UY44 / UY18



16VA



1. For STM705/706 only.
2. For STM813L only.

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias HTFB / HTGB High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

Test name	Description	Purpose
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

APPENDIX

Moisture Barrier Bag for 4-layer preplated frame NiPdAgAu for SO in ST Bouskoura

What is the change?

The reels and tubes of selected packages with Pre plated lead frames will be packed into a Moisture Barrier Bag (MBB).

The Moisture Barrier Bag will contain desiccant. The Label will be positioned on the MBB.

Once the MBB is removed, there is no change.



Why?

Moisture barrier bag will protect the product during exposure to uncontrolled environment before product usage (transportation/storage).

When?

The new packing of and 4-layer PPF Frame, for SO Assembled at ST Bouskoura (Morocco), will start from W23'16.

How will the change be qualified?

The packing with the MBB has been qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

Major steps of the qualification plan are:

- Workability
- Construction checking
- Reliability checking

What is the impact of the change?

- Form: No change
- Fit: No change
- Function: No change

List of products impacted by this change is attached to this notification.

How can the change be seen?

Change will be seen at unpacking.